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This one-year feasibility study explored the use of thermal dip-pen nanolithography (DPN) for the purpose of nanoscale electronics manufacturing. In this project, we have demonstrated that using the thermal DPN technique that both indium metal, and semiconducting organic materials (PDDT, PVDF) can be written in arbitrary locations on semiconductor surfaces with sub-100 nm feature sizes. We have measured the electrical properties of these nanostructure deposits and found them to be electrically functional. This accomplishment opens new opportunities for nanoelectronics manufacture and repair, where a functional deposit of an electronic material can be deposited in an arbitrary single location. Thus we can report success in this feasibility study.						
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## **FINAL REPORT FOR FA9550-06-1-0005**

Contract/Grant Title: FEASIBILITY STUDY OF NANOSCALE SEMICONDUCTOR MANUFACTURE USING THERMAL DIP PEN NANOLITHOGRAPHY

Contract/Grant #: FA9550-06-1-0005

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### **SUMMARY OF PROJECT ACCOMPLISHMENTS:**

This one-year feasibility study explored the use of thermal dip-pen nanolithography (DPN) for the purpose of nanoscale electronics manufacturing. In this project, we have demonstrated that using the thermal DPN technique that both indium metal, and semiconducting organic materials (PDDT, PVDF) can be written in arbitrary locations on semiconductor surfaces with sub-100 nm feature sizes. We have measured the electrical properties of these nanostructure deposits and found them to be electrically functional. This accomplishment opens new opportunities for nanoelectronics manufacture and repair, where a functional deposit of an electronic material can be deposited in an arbitrary single location. Thus we can report success in this feasibility study.

Further details are provided in the attached publications.

## Direct Writing of a Conducting Polymer with Molecular-Level Control of Physical Dimensions and Orientation

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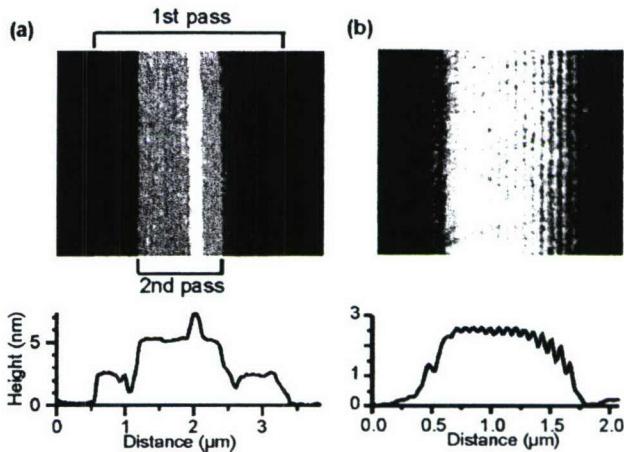
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Achieving the highest performance in organic electronic devices requires nanometer-scale control of the organic film structure.<sup>1,2</sup> For instance, field-effect mobilities in organic field-effect transistors depend strongly on the molecular ordering both within the organic film and with respect to the substrate. Although small organic molecules can be reliably deposited with nanoscale thickness control,<sup>3</sup> the fabrication of polymer nanostructures remains a significant challenge due to the large number of conformational degrees of freedom found in polymers. Conventional polymer deposition methods, such as spin-coating and vapor deposition, cannot control the polymer nanostructures, hampering improvements of polymer-based electronic devices. Herein we report a new technique for polymer deposition, thermal dip-pen nanolithography (tDPN),<sup>4</sup> that can write molecularly ordered polymer nanostructures with exquisite control of both physical dimensions and orientation. Using tDPN, we deposited poly(3-dodecylthiophene) (PDDT) nanostructures on silicon oxide surfaces with lateral dimensions below 80 nm and monolayer-by-monolayer thickness control from a single molecular monolayer ( $\sim 2.6$  nm) to tens of monolayers.

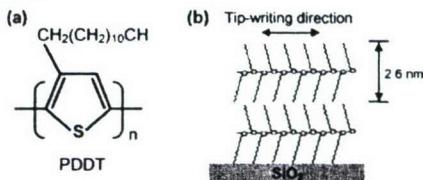
In tDPN, a custom-made atomic force microscope (AFM) cantilever with an integrated tip heater is precoated with an “ink” that is solid at room temperature. The ink is then precisely deposited onto a substrate surface when the tip temperature is set close to the ink’s melting temperature. The tDPN tip may be reproducibly heated within milliseconds up to 1000 °C,<sup>5</sup> well above the melting temperature of PDDT ( $T_m = 120$  °C<sup>6,7</sup>). PDDT (Scheme 1a) belongs to a class of conducting polymers, poly(3-alkylthiophene)s (P3ATs), that show great promise as active elements in organic electronics.<sup>2,8</sup> These polymers are chemically stable, soluble in common solvents, and easily processible.<sup>8</sup> Most importantly, they have shown some of the highest field-effect mobilities among conducting polymers (as high as  $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ).<sup>1,9</sup> Note that, to achieve such high mobilities, a high degree of molecular order is required in the film and at the interface between the film and the gate oxide ( $\text{SiO}_2$ ).<sup>1</sup>

Figure 1a demonstrates that a PDDT monolayer covering several square micrometers with relatively few defects can be easily deposited on room-temperature  $\text{SiO}_2$  by raster-scanning a PDDT-coated tip heated to 134 °C, above PDDT’s  $T_m$  but less than its degradation temperature of 175 °C.<sup>10</sup> (See Supporting Information for details on tip preparation.) Moreover, a subsequent scan over the first layer forms a second monolayer without disturbing the first one. A narrow third monolayer was also formed. The uniformity of the layers is manifested in the average height profile (Figure 1a). An analysis of the roughness (not shown) reveals that the roughness of the first two monolayers was comparable to (or less) than that of the substrate ( $r_{\text{rms}} = 0.22$  nm), suggesting a high degree of uniformity and order with the film.



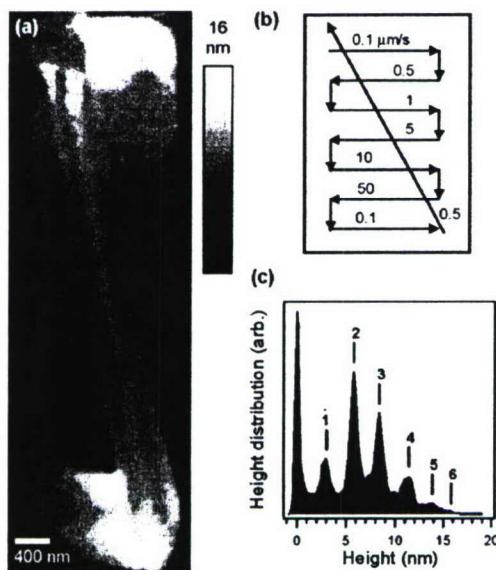
**Figure 1.** Tapping-mode AFM images of PDDT films deposited on  $\text{SiO}_2$ . The PDDT-coated tip was raster scanned from the top right to the bottom left at  $5 \mu\text{m/s}$  with  $47 \text{ nm per line}$  while it was heated at (a)  $134$  and (b)  $117$  °C. In (a), the outer square resulted from the first pass, which deposited a single monolayer. After  $50$  s, the second pass deposited a second monolayer without disturbing the first. Below is the average height for each of the scan lines. In (b) is shown the alignment of polymer strands parallel to the tip-writing (fast scan) direction. Below is the average height for each of the scan lines.

**Scheme 1.** (a) PDDT and (b) First and Second Monolayers of PDDT on  $\text{SiO}_2$



The thicknesses of the first three monolayers in Figure 1a are  $2.4$ ,  $2.7$ , and  $2.2$  nm, respectively. These thicknesses correspond closely to the PDDT interlayer spacing of  $2.6$  nm found in X-ray diffraction studies<sup>6</sup> of P3AT films. In these studies, the P3AT films were composed of submicrometer-size crystalline domains embedded in an amorphous matrix, with each crystalline domain having a lamella structure with  $\pi-\pi$  interchain stacking stabilizing two-dimensional sheets. On the basis of the thickness of the discrete layers, we conclude that our PDDT structures are composed of molecularly ordered, bulk-like lamella with the alkyl groups oriented perpendicular to the substrate (Scheme 1b). Note that this is the preferred orientation of the polymer to achieve a high field-effect mobility.<sup>1</sup> Although there have been several recent reports of scanning probe deposition of conducting polymers,<sup>11–15</sup> to our knowledge, our results are the first demonstration of nanoscale deposition of *molecularly ordered* polymer nanostructures with controlled thicknesses.

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**Figure 2.** (a) Tapping-mode AFM image of a PDDT film deposited on  $\text{SiO}_2$  at 134 °C. (b) The writing pattern with the respective  $v_{\text{tip}}$  ( $\mu\text{m/s}$ ). The  $v_{\text{tip}}$  for vertical lines was 1  $\mu\text{m/s}$ . (c) Height distributions of the PDDT nanostructures. The numbers represent the number of monolayers.

Depositing a single monolayer allowed us to investigate further the two-dimensional structure of PDDT self-assembly (Figure 1b). During this raster deposition, the tip temperature, 117 °C, was slightly below the PDDT melting temperature, but higher than its glass transition temperature, ~50 °C (and hot enough to initiate writing). These conditions create aligned polymer bundles  $73 \pm 4$  nm wide, equivalent to the width of ~190 PDDT strands. The bundles are much narrower than the average length of a PDDT strand (~500 nm), suggesting that the deposited polymer strands are aligned parallel to the fast-scan direction (Scheme 1b), possibly aided by mechanical combing<sup>16</sup> by the tip. Additional evidence of anisotropic alignment during single-pass deposition (with less combing) can be found in the Supporting Information. Anisotropic alignment of polymer strands can significantly improve electronic or optoelectronic devices. A recent study by Hoofman et al.<sup>17</sup> showed that the one-dimensional intrachain charge carrier mobility of an isolated conducting polymer is more than 3 orders of magnitude higher than that in bulk. Scanning tunneling microscopy analysis, currently underway, should further elucidate the structure and electronic properties of these highly ordered structures.

The thickness and morphology of the written structures are dependent on the writing speed and tip temperature. To study their dependence on the writing speed, a serpentine pattern was written at various writing speeds  $v_{\text{tip}}$ , ranging from 0.1 to 50  $\mu\text{m/s}$ , while the tip temperature remained constant. A representative AFM image of a pattern written on a  $\text{SiO}_2$  substrate at 134 °C is displayed in Figure 2a, with the corresponding height histogram shown in Figure 2c. Notice that the polymer is deposited in *discrete layers* (a total of six are observed in this pattern), similar to those observed during epitaxial film growth, with an average layer thickness of  $2.6 \pm 0.24$  nm. At this tip temperature, multilayered structures are deposited at the lowest  $v_{\text{tip}}$  (0.1  $\mu\text{m/s}$ ), a single layer is formed from 5 to 10  $\mu\text{m/s}$ , and a discontinuous pattern of single-layer islands is deposited at 50  $\mu\text{m/s}$ .

To study the effect of the tip temperature on the thickness and morphology, the pattern writing was repeated for tip temperatures slightly below and above that required for melting the bulk polymer (118 and 150 °C, respectively). At 118 °C, three monolayers are deposited at the slowest speeds, with average thickness  $2.8 \pm 0.23$

nm/monolayer; at 150 °C, up to 14 layers are formed with an average thickness of  $2.5 \pm 0.32$  nm/monolayer (Supporting Information). Multilayer structures can be built up by multiple depositions, as evidenced by the additional layers discretely deposited on the diagonal return path.

Controlling the temperature of the tip provides tDPN unique advantages over conventional DPN.<sup>18,19</sup> The higher deposition rate available allows tDPN to write polymer structures faster than conventional DPN. For example, to obtain a uniform film over a designated area, conventional DPN often requires multiple raster scans over the area.<sup>18</sup> Conventional DPN lines of conducting polymers suffered from discontinuity even at  $v_{\text{tip}} < 0.5 \mu\text{m/s}$ .<sup>14</sup> In contrast, tDPN can deposit a uniform PDDT monolayer in a single sweep at  $>10 \mu\text{m/s}$ . Increasing the polymer temperature during deposition may also accelerate the polymer ordering process. Finally, the low vapor pressure of the polymer inks used in tDPN should allow the deposition of polymer nanostructures in ultrahigh vacuum.

In summary, we demonstrate that polymer nanostructures can be directly written by tDPN with unprecedented control. The thickness can be controlled monolayer-by-monolayer, with each monolayer being aligned along the deposition direction and with respect to the surface. Line widths  $<80$  nm are also readily achieved (Supporting Information). The ability to write molecularly ordered polymer nanostructures offers opportunities not only to reliably investigate the intrinsic limit of charge transport in polymer nanostructures but also to integrate polymer-based components directly into conventionally fabricated devices. Finally, the capability of tDPN to control physical dimensions and molecular ordering may hold for other types of macromolecules.

**Acknowledgment.** This work was supported by the U.S. Office of Naval Research, the Defense Advanced Research Projects Agency, and an NSF CAREER award for W.P.K.

**Supporting Information Available:** Experimental procedures; anisotropic orientation of PDDT; height distributions of PDDT patterns at 118 and 150 °C; and a PDDT pattern with line width  $<80$  nm. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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# Direct deposition of continuous metal nanostructures by thermal dip-pen nanolithography

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We describe the deposition of continuous metal nanostructures onto glass and silicon using a heated atomic force microscope cantilever. Like a miniature soldering iron, the cantilever tip is coated with indium metal, which can be deposited onto a surface forming lines of a width less than 80 nm. Deposition is controlled using a heater integrated into the cantilever. When the cantilever is unheated, no metal is deposited from the tip, allowing the writing to be registered to existing features on the surface. We demonstrate direct-write circuit repair by writing an electrical connection between two metal electrodes separated by a submicron gap. © 2006 American Institute of Physics. [DOI: 10.1063/1.2164394]

Dip-pen nanolithography (DPN) is a scanning-probe based nanolithography technique that uses the probe tip like an inked pen, transferring a chemical “ink” coating from the probe tip to a surface through direct contact between the tip and surface.<sup>1</sup> Chemical inks deposited by DPN include thiols, biomolecules, sols, silanes, and nanoparticles.<sup>2</sup> DPN offers great promise because of its ease of use and resolution of 15 nm or better. However, conventional DPN requires inks that are mobile under ambient conditions, thereby incurring two significant limitations. First, the ink deposition rate from a given probe can only be affected by changing the ambient humidity or temperature or by heating the substrate,<sup>3,4</sup> making dynamic control of deposition difficult. Second, the inability to “turn off” deposition induces contamination or smearing if the inked probe performs pre- or post-deposition metrology. Thermal DPN (tDPN), shown in Fig. 1, overcomes these limitations by using a cantilever with an integrated heater to perform DPN with an ink that is solid at room temperature and flows only when melted at higher temperatures.<sup>5</sup> Deposition can be turned on and off by modulating heating power and, because the ink is solid at room temperature, an inked cantilever can image a surface or a deposit without contamination from depositing additional ink.

The requirement for inks to be mobile at room temperature in conventional DPN has led to an emphasis on organic self-assembled monolayer and biomolecular inks, with only a few efforts to write the electrically conducting nanostructures that would be required for nanoelectronics. Conducting polymers have been patterned electrochemically<sup>6–8</sup> and in a sol-like process,<sup>9</sup> and DPN of sols has generated magnetic and semiconductor nanostructures.<sup>10,11</sup> In forming metallic nanostructures, DPN has been used to deposit clusters of metal nanoparticles,<sup>12,13</sup> form etch resists on top of thin metallic films,<sup>14,15</sup> and act as a source of metal salt for electrochemical or electroless surface reduction.<sup>16–18</sup> Many applications, including nanometer-scale circuit fabrication and mask writing, require nanoscale deposition of continuous metal

films. However, to our knowledge, current DPN metallic deposition techniques have not demonstrated the single-step formation of a continuous metal layer on an arbitrary substrate.

In this letter, we describe the use of tDPN to perform nanoscale deposition of indium metal, using the heated AFM probe tip much like a nanometer-scale soldering iron. The cantilever registered the written deposit to previously fabricated structures and performed post-deposition metrology without contamination. Electrical measurements and Auger nanoprobe spectroscopy confirmed the electrical continuity and composition of the deposit. The direct deposition of metal demonstrates the feasibility of using tDPN for both structural and electrical deposition applications. To our knowledge, this letter reports the first demonstration of electrical transport through a DPN-deposited material without further processing.

The experiments used heatable silicon AFM cantilevers that were fabricated by our group using a standard silicon-on-insulator process.<sup>19</sup> Similar cantilevers have been developed for data storage.<sup>20</sup> The cantilever tip was fabricated on a microscale heater embedded in the cantilever, and had a radius of curvature of ~20 nm estimated from scanning electron microscopy. The cantilevers had a thermal time constant in the range of 1–10  $\mu$ s and a temperature-sensitive resistance that allowed temperature calibration.<sup>21</sup> The room temperature electrical resistance of the cantilevers was ~2 k $\Omega$ , with a peak resistance close to 7 k $\Omega$  when heated to 550 °C.

Indium was chosen as the deposition metal because of its relatively low melting temperature of 156.6 °C and its high wettability on many surfaces, including ceramics, glass, silicon, and metal oxides.<sup>22</sup> Indium was loaded onto the cantilever tip by bringing a clean tip into contact with a layer of In with a contact force of ~20 nN at room temperature, and then heating the cantilever. The cantilever temperature required to melt the indium near the cantilever tip depended strongly on the contact force. At contact forces of ~20 nN, a cantilever temperature >1000 °C was required to induce melting, while increasing the contact force to 1000 nN en-

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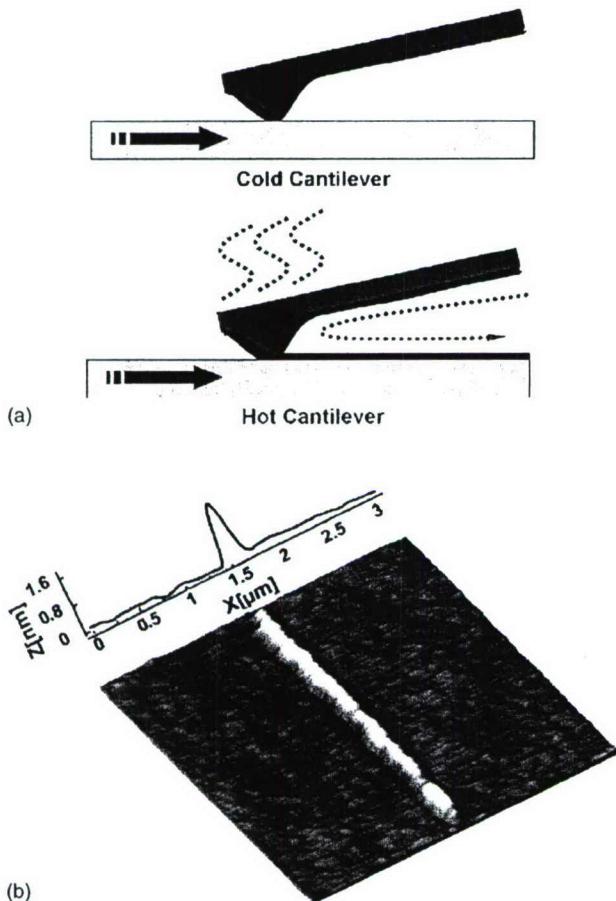


FIG. 1. (a) Schematic of the operation of tDPN, which uses a heated AFM cantilever with a tip coated with a solid "ink." When the tip is hot enough to melt the ink, it flows onto the substrate. No deposition occurs when the tip is cold, allowing imaging without unintended deposition. (b) A topographic AFM image of a continuous nanostructure deposited from an In-coated tip onto a borosilicate glass substrate.

abled melting with a cantilever temperature of  $500^\circ\text{C}$ . The thermal contact resistance between the cantilever and indium substrate was larger than the thermal resistance within the thermally conductive indium in contact with the tip, and thus the strong contact force-dependence of the cantilever temperature required to melt the indium substrate may be caused by the increased contact area between the tip and substrate.<sup>23</sup> Although increasing the tip-substrate contact force yielded improved thermal contact, high contact forces caused tip wear, reducing imaging and deposition resolution; therefore, contact forces were kept minimal. After melting was induced, the tip penetrated into the indium and the thermal resistance between tip and substrate was reduced, causing the cantilever temperature to decrease to roughly half of its value at low contact force before melting. Despite the decreased cantilever temperature, the In substrate would remain melted after tip penetration. Successful loading of indium onto the cantilever occurred by scanning the tip on an indium substrate with a contact force of  $500 \text{ nN}$  at  $6 \mu\text{m/s}$  while heating the cantilever at  $13.4 \text{ mW}$ , or  $\sim 1030^\circ\text{C}$ . After loading, the tip was pulled out of contact with the indium and the cantilever heat was turned off.

The indium-coated cantilever could redeposit indium onto another surface by simply reheating the cantilever while the tip was in contact with the second surface. Scanning the

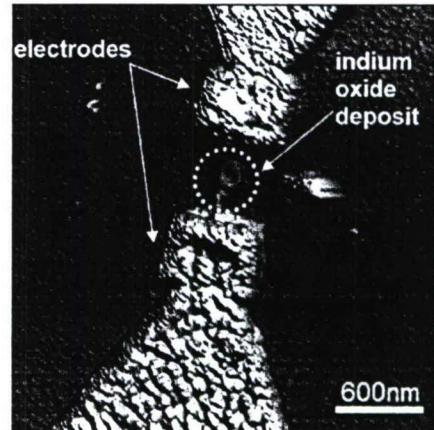


FIG. 2. Topographical AFM image of a continuous structure deposited with In across a  $500 \text{ nm}$  wide gap (circled) between pre-fabricated gold electrodes.

tip while heating produced continuous lines of deposited indium, an example of which is shown in Fig. 1. The dimensions of the deposited line depended on the tip loading, deposition temperature, deposition speed, and the number of repetitions along the deposition line. We have deposited continuous lines over a wide range of conditions, from  $250\text{--}800^\circ\text{C}$ ,  $0.01\text{--}18 \mu\text{m/s}$ , and  $32\text{--}128$  raster scans, and on substrates of borosilicate glass, quartz, silicon with a native oxide, and  $1 \mu\text{m}$  thick thermally grown silicon oxide on silicon. Deposited lines ranged from  $50$  to  $300 \text{ nm}$  in width and from  $3$  to  $12 \text{ nm}$  in height. The thickness to width ratio never exceeded unity. Repeated imaging with a cool indium-coated tip had no effect on the deposited lines, and contamination, spreading, or loosening of the deposited indium was never observed.

To test the electrical continuity and transport properties of the deposited indium, a substrate with gold electrodes separated by a  $500 \text{ nm}$  gap was fabricated by e-beam lithography onto a  $100 \text{ nm}$  thick silicon oxide film on a silicon substrate. Before heating the cantilever, the indium-coated tip was used to image the electrode and locate the gap. To deposit indium across the gap, the tip was heated with  $5.34 \text{ mW}$ , or  $425^\circ\text{C}$ , and the tip scanned along a  $2 \mu\text{m}$  line spanning the gap at  $4 \mu\text{m/s}$ . After scanning the line continuously for  $32 \text{ s}$ , the resulting deposit was  $5 \text{ nm}$  tall and had a width varying from  $100$  to  $200 \text{ nm}$ . (See Fig. 2).

Chemical and electrical analyses of the nanostructures were performed in a unique ultrahigh vacuum (UHV) instrument combining a scanning electron microscope (SEM), a scanning Auger nanoprobe, and a four-tip nanoprobe capable of making *in situ* transport measurements across structures  $<1 \mu\text{m}$  long. As shown in Fig. 3, Auger electron spectroscopy performed directly on the nanostructure demonstrates that the deposit was pure indium oxide. Because the height of the deposit was less than the  $\sim 10 \text{ nm}$  thickness of the native oxide of indium, it is likely that the deposited indium was completely oxidized before electrical measurements could be performed, as the deposition was performed in air. Although not as conductive as indium, indium oxide is a conductor and has applications in molecular electronics and sensing.<sup>24</sup> Current-voltage ( $I\text{--}V$ ) measurements were made by contacting Pt probes to the Au electrodes connected by the indium deposit. As shown in Fig. 4, the linearity of the

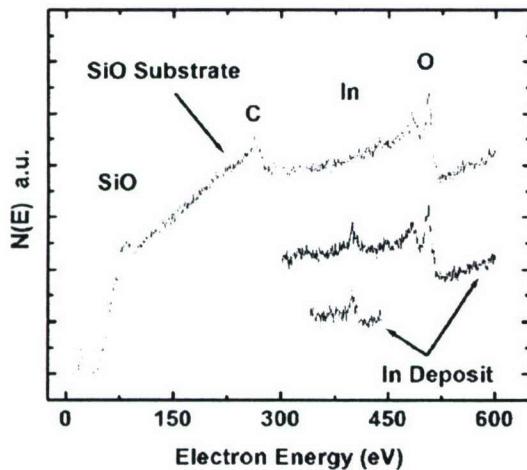


FIG. 3. Auger electron nanoprobe spectra collected at two different locations on the nanostructure and on the adjacent silicon oxide substrate demonstrating that the structure is indium oxide. Note that the spectra are displayed as total electron count,  $N(E)$ , not  $dN/dE$ .

$I-V$  measurement demonstrates that the deposit is continuous and ohmic, with a resistivity of  $2.5 \times 10^4 \Omega\text{-cm}$ . Note that no electrical conduction was observed between electrodes without indium deposits.

The electrical resistivity of indium oxide depends strongly on the deposition conditions, with reported values ranging from  $10^{-4}$  to  $10^8 \Omega\text{-cm}$ , making the measured resistivity within the reported range.<sup>25,26</sup> Amorphous indium oxide films have shown higher resistivity than polycrystalline films,<sup>25</sup> and poor crystallinity has resulted from indium oxide film deposition at low temperatures.<sup>25,26</sup> Since the silicon substrate was not independently heated during our experiment, the deposited liquid indium would be rapidly quenched as it flowed from the hot tip to the cool substrate. Rapid quenching would lead to a more disorganized film, which is consistent with the high measured resistivity. We are working to preserve the highly conductive metallic indium by depositing thicker wires that would not completely oxidize and performing the deposition in UHV (another notable capability of tDPN). Furthermore, a deep understanding of the interplay between the tip, ink, and the temperature field within the substrate will allow thermal engineering of the substrate

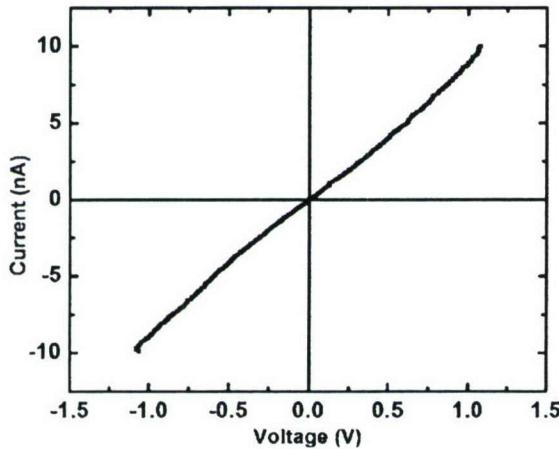


FIG. 4. Electrical transport through the nanowire structure shown in Fig. 2, demonstrating it is continuous and ohmic.

and, therefore, provide greater deposition control.

The direct writing of electrically continuous nanowires significantly expands the capabilities of DPN. This nanosoldering requires the combined metrology and lithography capabilities of tDPN and could not be performed with conventional DPN. The ability to deposit locally a solid metal could enable the direct prototyping of nanoelectronics or masks. Moreover, deposition could be coupled with AFM surface metrology to perform *in situ* inspection and repair of nanoelectronics. Finally, this technique could be easily performed in parallel using the extensive cantilever arrays already demonstrated, which could be pre-coated with In during fabrication.<sup>20</sup>

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